Telephone Ring Generator Controller

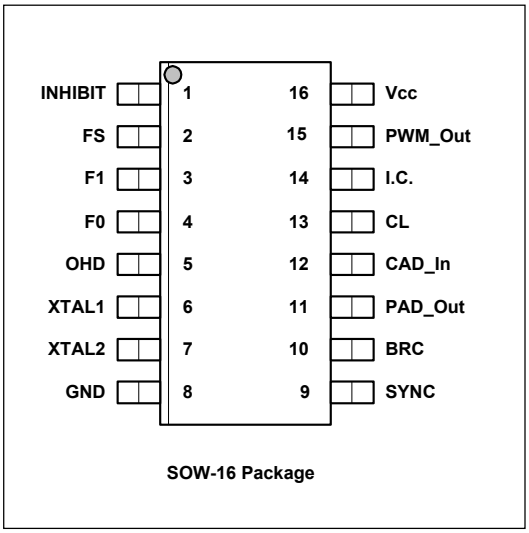
PD5036

US Patent No. 5,828,558
Patent Pending in Europe, and Asia

PD5036
TELEPHONE RING GENERATOR CONTROLLER

FEATURES

- Integrated Overload and Short Circuit Protection
- Programmable Large Swing Output Amplitude
- Digitally Selectable Ringing Frequencies; 16.7/20/25 or 50Hz
- Line Regulated Output Amplitude, 45-93Vrms
- Overload Protection with Adaptive Output Amplitude
- Off-Hook / Overload Detection
- Zero Crossing Synchronization Output
- Operates from a Single 5V Supply
- Open Loop Flyback Topology Reduces Component Count
- Total Bill of Material Cost as Low as $5 Including the PD5036 for 2W Ring Generator Applications



SOW-16 Package

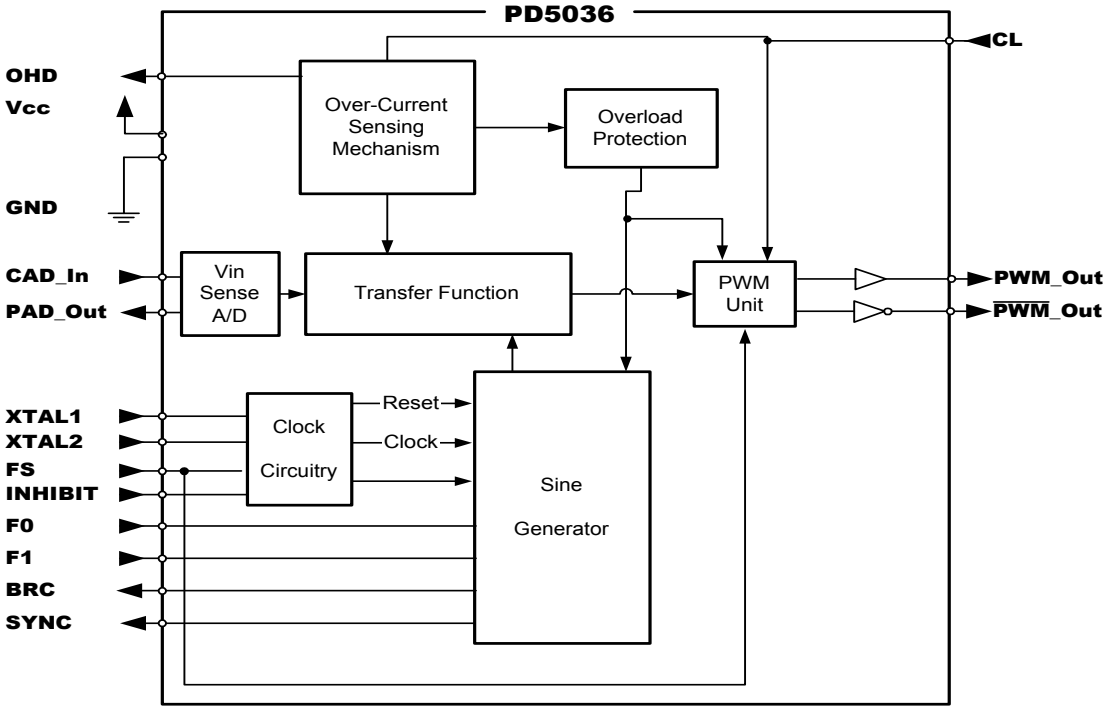
APPLICATIONS

- 1 to 3 Watt Low Cost Sine Wave Ring Generators
- 3 to 6 Watt advanced Sine Wave Ring Generators
- Large Variety of Customized Sine Wave Ring Generators
- Ring Generator for PBX, PABX, DCL, CTI and Key Systems
- Ring Generator for Rural Telephony and Wireless Local Loop Systems
- Ring Generator for Short/Long Loop Applications
- Ring Generator for Telecom Test Equipment

GENERAL DESCRIPTION

The PD5036 is a unique pulse width modulator controller, designed primarily for a variety of high voltage sinusoidal telephone ring generator applications. The PD5036 is suitable for applications requiring up to 6 Watt and provides all necessary controls for implementing advanced overload protection, zero crossing relay switching synchronization, Off-Hook detection, multiple ringing frequency selection and output amplitude adjustment.
The power train, designed to be used with the PD5036, is an isolated, open loop flyback topology. The PD5036 generates a PWM signal, which drives a FET transistor that switches the primary of a flyback transformer. This produces a rectified half sine wave on the secondary side of the transformer. An additional control signal synchronizes a 4-output transistor bridge, which converts the rectified half sine wave to full sine wave. In order to maintain the ring generator's input to output isolation, the synchronization signals control the bridge via an opto coupler pair. The controller also includes overload protection, A/D function for measuring the input voltage, and a report signal for indicating over current.
The PD5036 is a cost-effective solution for applications using more than 10,000 units. For quantities less than 10,000 units, the most economical solution is a modular sine wave ring generator (PCR-SIN01A *Series*, PCR-SIN03B *Series*, or the PCR-SIN06 *Series)*.

INTERNAL BLOCK DIAGRAM



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PIN DESCRIPTION

Pin	Symbol	Function
1	INHIBIT	Remote On/Off and Reset Control. (Referenced to GND terminal)
2	FS	PWM output frequency selection input.
3	F1	Ringing frequency selection input.
4	F0	Ringing frequency selection input.
5	OHD	Off-Hook/Overload reporting output.
6	XTAL1	Oscillator's high gain amplifier input. Crystal or ceramic resonator or an external clock source may be applied.
7	XTAL2	Oscillator's amplifier output. Required when a crystal or a ceramic resonator is used. This terminal should be left unconnected when using an external clock source.
8	GND	Ground terminal.

Pin	Symbol	Function
9	SYNC	Ringing signal zero crossing induction output. (2-2.5ms before crossing)
10	BRC	Bridge synchronization control output.
11	PAD_Out	A/D reference control signal.
12	CAD_In	Input signal from the external A/D comparator. (Optional line regulation circuit)
13	CL	Current Limit pulse counter input.
14	$\overline{\text{PWM\_Out}}$	Watchdog Output.
15	PWM_Out	Main PWM output signal.
16	VCC	5V DC Supply voltage.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
Vcc	DC Supply Voltage (Referenced to GND)	-0.5 to 6	V
CAD_In, FS, INHIBIT, F0, F1, CL, XTAL1, XTAL2.	DC Input Voltage (Referenced to GND)	-0.5 to Vcc+0.5	V
Tstg	Storage Temperature	-40 to 125	°C

Note: These are stress ratings. Exposure of the device to any of these conditions may adversely effect long-term reliability. Proper operation other than those specified in the ELECTRICAL SPECIFICATIONS is not implied.

ELECTRICAL SPECIFICATIONS

Unless otherwise stated, these specifications apply for: Vcc = +5V, $0°C \le T_A \le +70°C$.

DC CHARACTERISTICS

Pin Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	4.75		5.25	V
	Input Current @ Continuous			35	mA
	@ Surge of 200nsec every 3μsec			110	mA
GND	Output Current @ Continuous			50	mA
	@ Surge of 200nsec every 3μsec			125	mA
INHIBIT	Schmitt Trigger Input				
	Input Voltage Level VT+	2.65		3.35	V
	VT-	1.35		1.95	V
	Internal Pull Down		100		KΩ
F0 , F1	CMOS 5V Input Buffer				
	Input Voltage High Level	0.7•Vcc	5	Vcc+0.5	V
	Input Voltage Low Level	-0.5	0	0.3•Vcc	V
	Internal Pull Up		100		KΩ
FS	Schmitt Trigger Input				
	Input Voltage Level VT+	2.65		3.35	V
	VT-	1.35		1.95	V
	Internal Pull Down		100		KΩ
BRC	Output Source Current @ 4.5v		5	10	mA
	Output Sink Current @ 0.5v		5	10	mA
SYNC	Output Source Current @ 4.5v		1.5	2	mA
	Output Sink Current @ 0.5v		5	10	mA
OHD	Output Source Current @ 4.5v		1.5	2	mA
	Output Sink Current @ 0.5v		5	10	mA
PWM_Out	Output High Level @ Iout=20 mA	Vcc-0.5			V
	Output Low Level @ Iout=-20 mA			0.5	V
	Output Source/Sink Current				
	@ Continuous		20		mA
	@ Surge of 200nsec every 3μsec			48	mA

Pin Symbol	Parameter	Min	Typ	Max	Units
WDO	Output High Level @ Iout=1mA Output Low Level @ Iout=-1mA Output Source/Sink Current @ Continuous	Vcc-0.5	 1	 0.5 	V V mA
PAD_Out	Output High Level Output Low Level Output Source/Sink Current	Vcc-0.2 1.5	 	 0.2 2	V V mA
CAD_In	CMOS 5V Input Buffer Input Voltage High Level Input Voltage Low Level internal Pull Up	 0.7•Vcc -0.5	 5 0 100	 Vcc+0.5 0.3•Vcc 	 V V KΩ
CL	CMOS 5V Input Buffer Input Voltage High Level Input Voltage Low Level internal Pull Up	 0.7•Vcc -0.5	 5 0 100	 Vcc+0.5 0.3•Vcc 	 V V KΩ

CLOCK CHARACTERISTICS

Pin Symbol	Parameter	Min	Typ	Max	Units
XTAL1 XTAL2	Oscillator Input Pad Oscillator Output Pad				
	Clock Frequency Total Frequency Accuracy	10		20 1	MHz %
	(Total Frequency Accuracy is identical to the Crystal/Ceramic Resonator or external clock source frequency accuracy) The Clock Oscillator works with a Crystal or a Ceramic Resonator or an external clock source.				

OPERATING TEMPERATURE

Symbol	Parameter	Min	Typ	Max	Units
T_A	Ambient temperature	-40	25	85	°C
Tj	Maximum Junction Temperature			125	°C

OUTPUT RINGING & PWM FREQUENCIES

Oscillator Frequency (Main Clock)	FS	F1	F0	PWM Frequency	Output Frequency	Output Frequency Accuracy
12.28MHz	0	0	0	96KHz	50Hz	2% max.
	0	0	1	96KHz	16.7Hz	2% max.
	0	1	0	96KHz	25Hz	2% max.
	0	1	1	96KHz	20Hz	2% max.
19.66MHz	1	0	0	307.2KHz	50Hz	2% max.
	1	0	1	307.2KHz	16.7Hz	2% max.
	1	1	0	307.2KHz	25Hz	2% max.
	1	1	1	307.2KHz	20Hz	2% max.

INHIBIT OPERATION

Operating State	Inhibit State
Output Enabled	0
Output Disabled	1

INHIBIT OPERATION DELAY

F S	Inhibit Input	Operating State	Inhibit Response Time
X		Output Enabled	40mS typical
0		Output Disabled	Wait for end of ½ sine cycle, 30mS maximum
1		Output Disabled	Immediate

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SYNC OUTPUT

F1	F0	Output Frequency	SYNC Pulse Width mS
0	0	50	4
0	1	16.7	5
1	0	25	5
1	1	20	5

INPUT VOLTAGE SAMPLING A/D CONVERTER

Unless otherwise stated, these specifications apply for: Vcc = +5V, -40C° ≤ T_A ≤ +85°C, PAD_Out current ≤ 3mA.

INTERNAL FUNCTIONAL PARAMETERS

Main Clock	A/D Resolution	A/D PWM Frequency PAD_Out	CAD_In Sampling Rate	Vsample Sensitivity	Full Scale Response Time
19.66MHz	8 bit	76.77KHz	9.6KHz	58.6mV	24.89mS
12.28MHz	8 bit	47.97KHz	6.0KHz	58.6mV	39.83mS

A/D BEHAVIORAL PARAMETERS

Symbol	Parameters	Min	Max	Units
A/D input operation voltage	Normal A/D operation	0.332	4.98	Vdc
(Vsample)	A/D not used*	0	0.293	Vdc

*CAD_In = "0" AND THE A/D REACHED ITS MINIMUM OPERATION VALUE (Minimum A/D Duty Cycle).

PWM UNIT

OPERATING RANGE

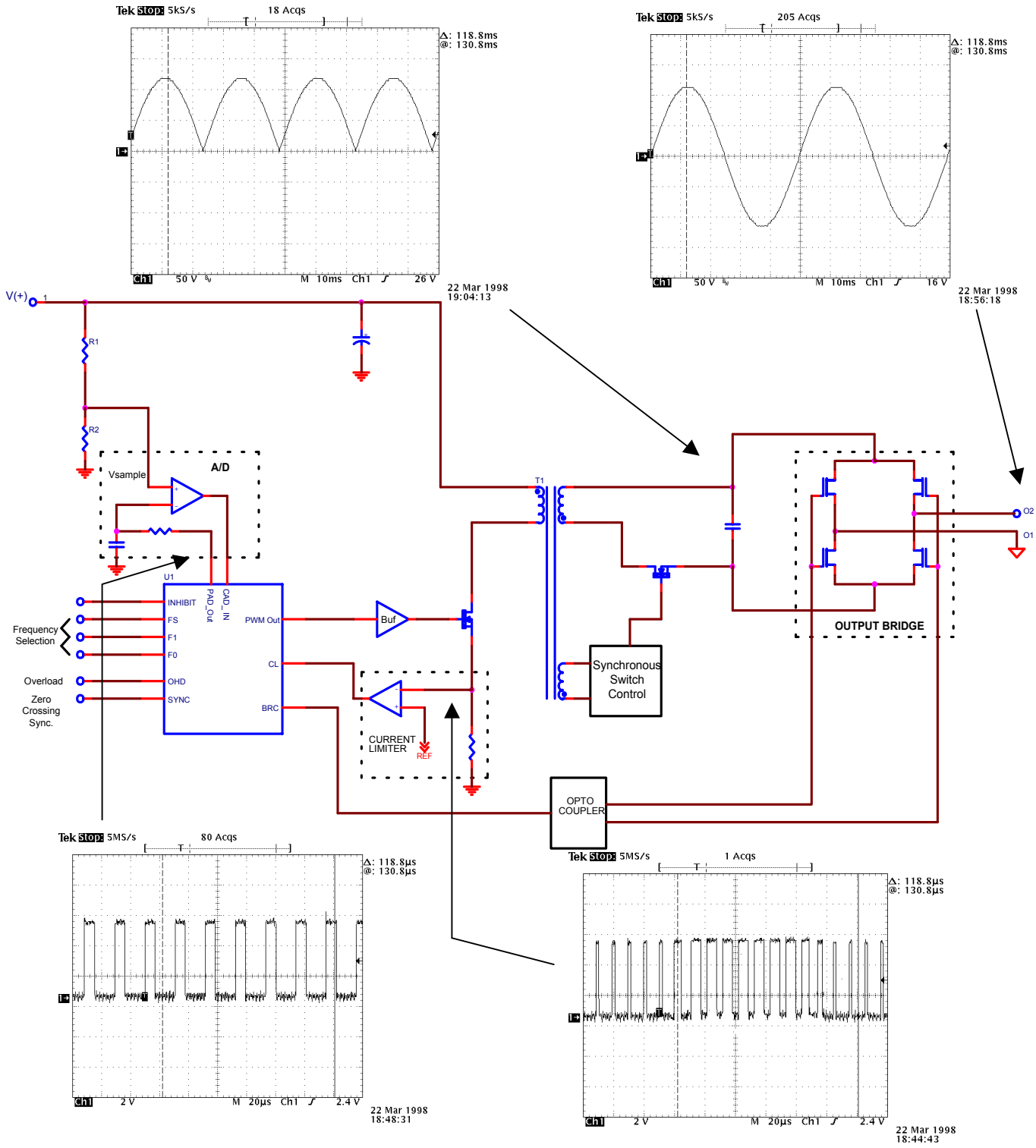
CL Input = '1'

Main Clock	FS	Output PWM Frequency	PWM Resolution	PWM Duty Cycle * Min	PWM Duty Cycle * Max
12.28MHz	0	96KHz	7 bit	0%	92.18%
19.66MHz	1	307.2KHz	6 bit	0%	92.18%

*Duty Cycle = Ratio between the time the signal's On duration to the On + Off duration.

PWM UNIT OPERATION AT OVERLOAD CONDITION

	PWM Turn Off Delay When CL	PWM Turn Off Delay When CL ↘	
FS	Main Clock	Min	Max
0	12.28Mhz	1 Main Clock 81.43ns	2 Main Clocks 162.86ns
1	19.66Mhz	1 Main Clock 50.86ns	2 Main Clocks 101.72ns



Typical Operating Circuit

DETAILED DESCRIPTION

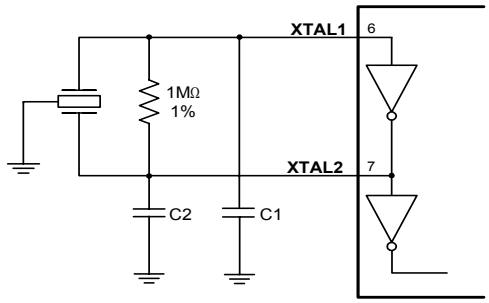
CLOCK

XTAL1, XTAL2: The oscillator generates the internal PD5036 clock frequency.
A Crystal, Ceramic Resonator, or an external clock source may be used to generate the clock's basic frequency.
When a Crystal or a Ceramic Resonator is used, it should be connected between XTAL1 and XTAL2 terminal. For an external clock source, connect the source to XTAL1, leaving XTAL2 unconnected.
When using a Ceramic Resonator, use the product's specification connection recommendations.
When using a Crystal or Ceramic Resonator, a 1Mohm 1% bias resistor *must* be connected in parallel.
C1 and C2 recommended values for the different frequency sources are specified in the table below.

Oscillator type	Frequency	C1	C2
Crystal	12.28MHz	22pF	22pF
Crystal	19.66MHz	10pF	10pF
Ceramic Resonator	12.28MHz	10pF	56pF
Ceramic Resonator	19.66MHz	10pF	56pF

When using an external clock source, C1 and C2 and the Resistor should not be installed and XTAL2 should be left open.

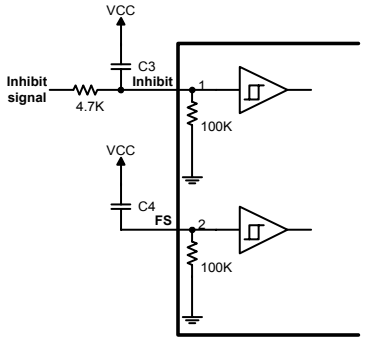
For the oscillator frequency, refer to the OUTPUT RINGING & PWM FREQUENCIES Table.



Oscillator Typical Configuration

TURN ON RESET OF THE PD5036

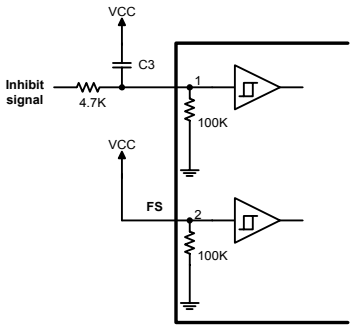
For proper operation, the PD5036 controller must be reset after power is applied. Reset is performed by setting the Inhibit and the FS terminals to a high logic level for longer than 1μ sec.
The Inhibit and the FS terminals are connected to an internal Schmitt input buffer with an internal 100KOhm pull down resistor.
To enable Power On Reset (POR) and proper inhibit operation, a series resistor and pull up capacitors must be connected to the INHIBIT terminal. The value of the resistor and the pull up capacitors determine the reset duration, and delay of the inhibit operation.



100KHz PWM Output POR Configuration

The value of C3 and C4 will be determined according to the Supply Voltage Rise Time and the Inhibit delay operation.

When using a 100KHz PWM output configuration the value of C4 should be 20 times smaller than C3.
[τ (FS) < τ (Inhibit)].



300KHz PWM Output POR Configuration

INHIBIT: The Inhibit input serves to turn the device's output On/Off by using digital control levels.
High logic level ("1") disables the device's output.
When the 96KHz configuration is utilized (FS="0"), the Inhibit shut down response is internally delayed until the end of the current half sine cycle, to the nearest output zero crossing.
When the 307KHz configuration is utilized (FS="1"), the Inhibit shut down response is immediate.

FS: This line selects between 96KHz and 307KHz main PWM frequency.
FS= "0" = 96KHz
FS= "1" = 307KHz
The 96KHz PWM frequency is suitable for medium power sine wave generators, with synchronous switching at the secondary.

In low cost, low power, ring generator applications, the synchronous switching circuitry may be eliminated. In order to maintain reasonable efficiency while not employing synchronous switching, the 307KHz PWM frequency is employed.

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FREQUENCY SELECTION

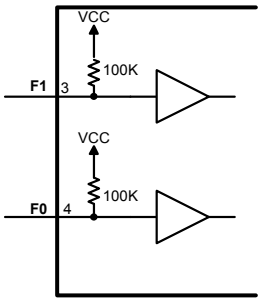
F0, F1: Selection of a single output ringing frequency between the four available options of 16.7, 20, 25 or 50Hz is achieved by the F0 and F1 inputs.

The state of F0 and F1 inputs must be set and stable prior to powering the PD5036. Changing the input state while the PD5036 is operating may not effect the output frequency, and may cause the controller to become unstable state.

The frequency selection should be made according to the OUTPUT RINGING & PWM FREQUENCIES table on page 45.

These inputs are CMOS standard and can be driven directly from CMOS components, or the frequency selection can be achieved by tying them to GND or Vcc.

Note: The PD5036 operation may be affected by *excessive noise surges* on F0 and F1 terminals while operating.



Frequency Selection Inputs

LINE REGULATION (A/D UNIT)

The ring generator circuit design is based on an open loop flyback topology. In order to regulate the output for input voltage changes, a forward compensation mechanism is used.

This mechanism is based on a digital sampling of the input voltage by the A/D unit, and correction of the main PWM duty cycle according to the internal transfer function.

The input voltage is sampled by an 8bit A/D unit, which is composed of external analog components and the internal PD5036 logic.

The internal portion of the A/D generates a PWM signal (PAD_Out) with a changing duty cycle according to the voltage sampled by the CAD_In terminal.

The sampled input voltage information influences the ringer output voltage amplitude in such a way that changes in Vin generates only a small change in Vout.

PAD_Out: PWM output for the external A/D circuit. The PWM frequency is the oscillator frequency divided by 8.

This line is connected to an external Low pass network that averages the PWM pulses to a DC voltage. The level of this DC voltage is proportional to the duty cycle of the PWM signal. The Low pass network is connected to the negative input of an external comparator. This DC voltage tracks the sampled voltage that is connected to the positive input of the comparator. If the DC voltage is lower than the sampled voltage, the internal A/D circuit will increase the PWM duty cycle. This will increase the DC level. The opposite happens when the sampled voltage is lower than the DC voltage.

CAD_In: This input line should be connected to the output of the A/D circuit's external comparator. CAD_In = "1" will increase the PWM duty cycle at the PAD_Out line. CAD_In = "0" will decrease the PWM duty cycle at the PAD_Out line. When the sampled voltage is stable, the A/D PWM duty cycle will change up and down by 1 bit and the comparator output will vibrate. These 1-bit vibrations are ignored by the A/D.

Applications that use highly regulated power supplies may eliminate the A/D external portions. In this event, the CAD_In should be permanently connected to GND. Note that no output voltage regulations based on input voltage changes will be performed.

LOW PASS NETWORK

The network is connected between the PAD_Out and the negative input of the comparator, built from R3 & C1.

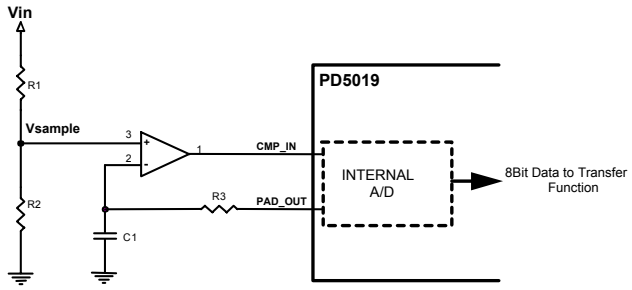
The low pass network is designed to average the PWM signal into a DC Level. This DC level is compared to the sampled voltage.

It is recommended to calculate the Low Pass network components values according to the following:

τ(Recommended) = C1 • R3 = 89.1mS @ 96KHz Operation

τ(Recommended) = C1 • R3 = 52mS @ 307KHz Operation

* For timing details refer to A/D CONVERTER, INTERNAL FUNCTIONAL PARAMETERS TABLE.



A/D Circuit Implementation

- The comparator inputs for the A/D function must operate in the range of 0 to 5V.
- The Vsample sampling is synchronized for the sine wave peak.

Voltage Divider: The voltage divider connects to the positive input of the comparator and is built of R1 & R2.

The voltage divider is required when an input voltage, Vin, higher than 5V is used. Design the Vsample voltage divider to deliver 2.5V for typical Vin Value is recommended.

OUTPUT PROTECTION MECHANISM

The overload and short circuit protection mechanisms support three protection levels:

1. Immediate pulse by pulse, input current limiting.
2. Power reduction, by output amplitude reduction.
3. Shut down for limited periods, to reduce heat dissipation.

The input of the protection unit is the CL input, connected to external current sense circuit output.

CL - Current Limiting Pulse Counter:

When the CL input changes to a Low due to excessive switch current, the PWM output immediately changes to Low until the end of the current PWM cycle. This will terminate the current through the switching FET and the CL input will return to a high level.

Output Amplitude Reduction Mechanism

During overload conditions, the PD5036 reduces the circuit output voltage, while maintaining a clean sine wave, to a level that delivers the allowed maximum output power. The protection unit counts the number of CL pulses which are received during a single half sine wave cycle and compares the result to an internal threshold. The numbers of CL pulses that exceed the threshold indicate overload conditions. Reduction of the output sine wave amplitude, in one step resolution, is accomplished according to the following equation.

$$\text{Vout peak} = \text{VpeakNominal} \times \frac{16}{\text{Step}}$$

During normal operating conditions, the step number is 16. In overload conditions, the step number can reach 31.

The amplitude can be reduced to about half of the nominal amplitude.

In each step there will be less current limit indications.

If the overload is removed and there are no CL pulses at all, the amplitude will begin to rise back, step by step. Each step takes one half of a sine wave cycle.

The OHD Output that reports an overload situation is activated based on the step number.

Reduction of the output amplitude, by more than 16 table steps, will be indicated by OHD change to High ("1").

When the protection unit raises the amplitude back to step 16, the amplitude will remain at this step at least a single sine period and this line will go back to Low ("0").

- High level (OHD="1") means the output is overloaded.
- Minimum pulse length = 1 sine cycle.
- Maximum time for Over Load detection = ½ sine cycle time, (30mS at 16.7Hz ringing frequency).
- Over load required duration, for detection = ½ sine cycle time.

This line can be useful for overload problem reports in medium size ringers, and can be used for off hook detection in small size ringers when there are few telephones connected to one line.

Output Shut Down

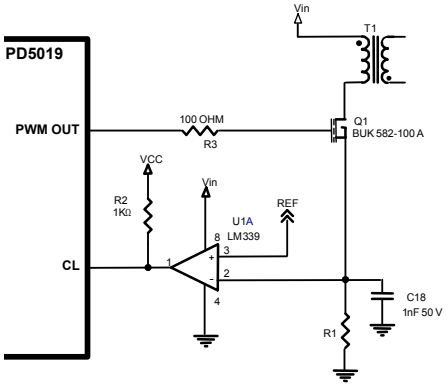
If the output load of the ring generator is high, and the output amplitude has reached its minimal level, an internal counter will start to count 300mS.

If the overload has not been removed after 300mS, the protection will shut down the PWM for 4.86 sec.

After the shutdown period, the PD5036 will begin operating at minimum amplitude level.

If there are still CL pulses, the internal counter will start to count 300mS again and shut down for 4.86 sec again.

However if the load is removed after the shutdown period, the output amplitude will start to increase, step by step.



Typical current sense circuit configuration

- Maximum amplitude reduction/incremental response time = ½ sine cycle time.
- Time for overload shut down = (8 • sine cycle time)+300mS. Max.
- Shut down period = 4.86Sec.

Timing accuracy is derived from the main oscillator frequency accuracy.

DETERMINING THE OUTPUT AMPLITUDE

The topology of the ring generator is an open loop flyback. In this topology, the output amplitude is determined by the PWM duty cycle.

The PD5036 changes its PWM duty cycle according to an internal sine wave reference table and a known mathematical transfer function.

To determine the maximum amplitude of the output sine wave, use the following equation:

$$\text{Vout}_{rms} = (2.773 \bullet n) \bullet (\frac{R1 + R2}{R2})$$

- R1 and R2 are the voltage divider resistors used in the Vin sampling A/D.
- **n** is the winding turn ratio of the transformer.
- It is recommended to change the output voltage amplitude by changing R1 or R2 while using the typical rated **n**. A high-resolution potentiometer can be used to obtain the proper resistor values during the circuit design.

CHOOSING **n**:

1. Define the input voltage range.
2. Calculate the average input voltage according to the following equation.

$$\text{Vin mid} = \frac{\text{Vin min} + \text{Vin max}}{2}$$

3. Choose the parameter **nVin** according to the following table.

Parameter	Min.	Recommended	Max.
nVin	42	48	54

4. Calculate **n** (winding turns ratio) according to the following equation.

$$\mathbf{n} = \frac{\text{nVin (choosed from the table)}}{\text{Vin mid}}$$

ADJUSTING OUTPUT AMPLITUDE WITHOUT A/D

When the input voltage sampling the A/D is not used (CAD_In = "0"), the maximum output amplitude is determined according to the input voltage and turns ratio.

$$\text{Vout rms} = 1.4731 \bullet \mathbf{n} \bullet \text{Vin}$$

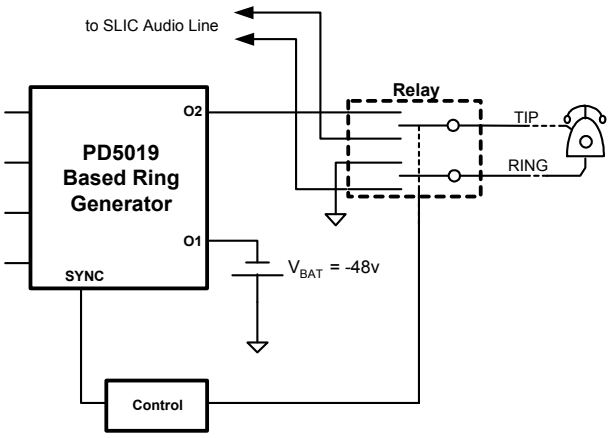
Note: When the input voltage sampling A/D is not used, the CAD_In terminal must be grounded.

PWM_Out: This is the PWM output signal. This output is capable of directly driving a FET.

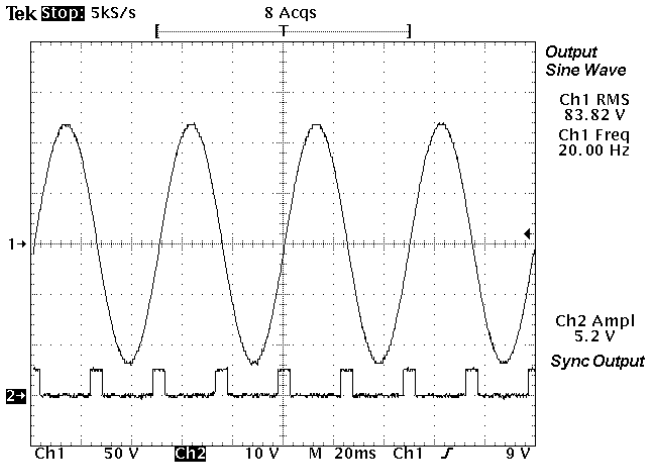
SYNCHRONIZATION SIGNALS

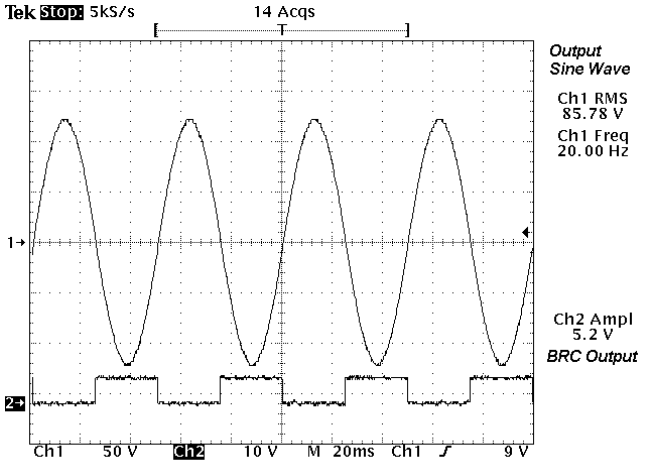
BRC: The BRC output controls the ring generator's output power bridge. The bridge converts the half sine rectified wave to a full sine wave at the output.
The BRC signal is a logic level square wave at the same frequency of the output sine wave.

SYNC: The SYNC output is used to synchronize output ringing relays switching with the ring generator's output voltage zero crossing. The SYNC output produces a high logic level pulse to indicate zero crossing. The SYNC pulse rises a short time prior to the output signal's zero crossing in order to allow for the relay response time. Exact signal timing are indicated in the ELECTRICAL CHARACTERISTICS SYNC OUTPUT parameters.



Zero crossing relay control utilizing the SYNC output



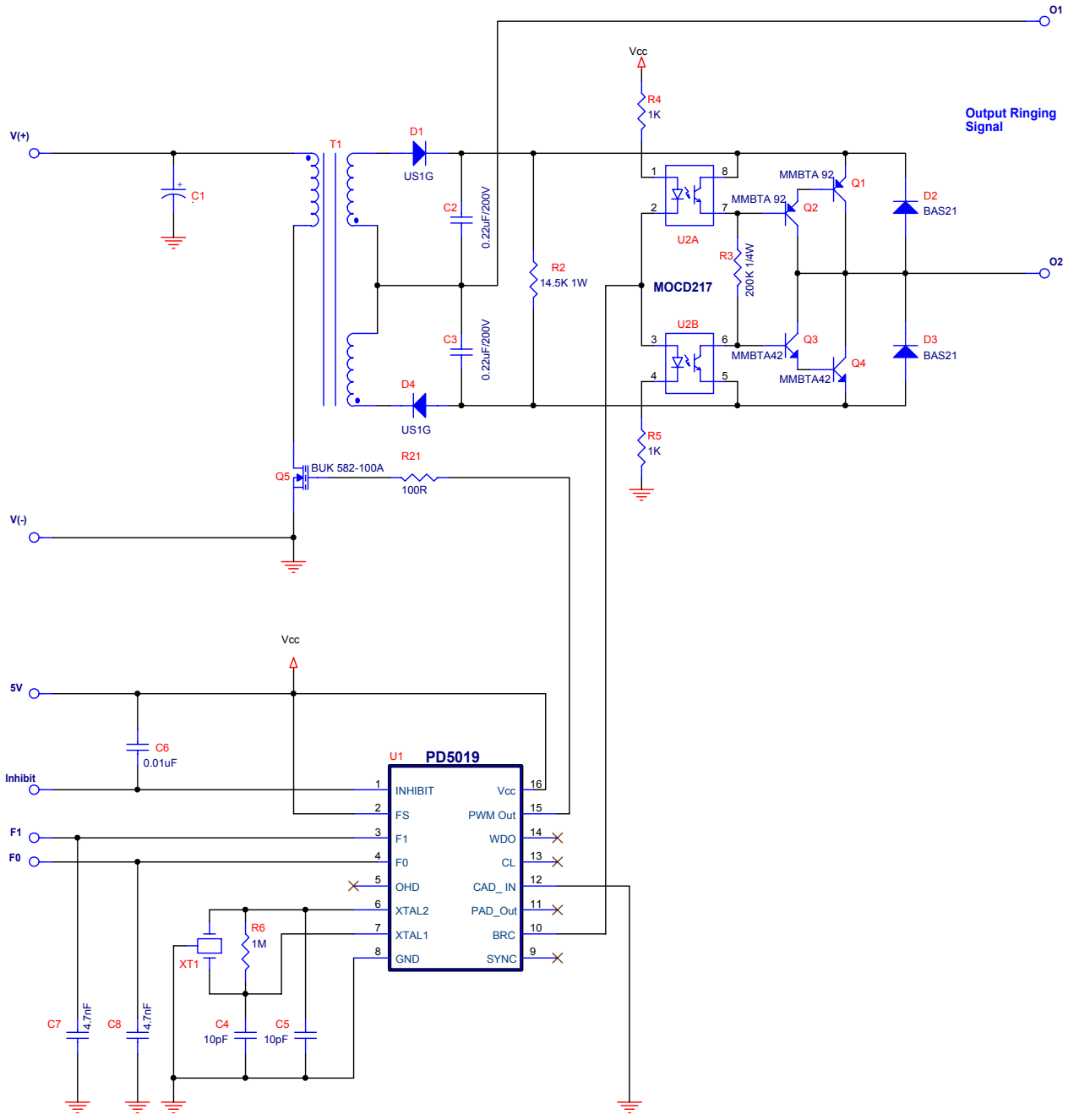


LOAD REGULATION

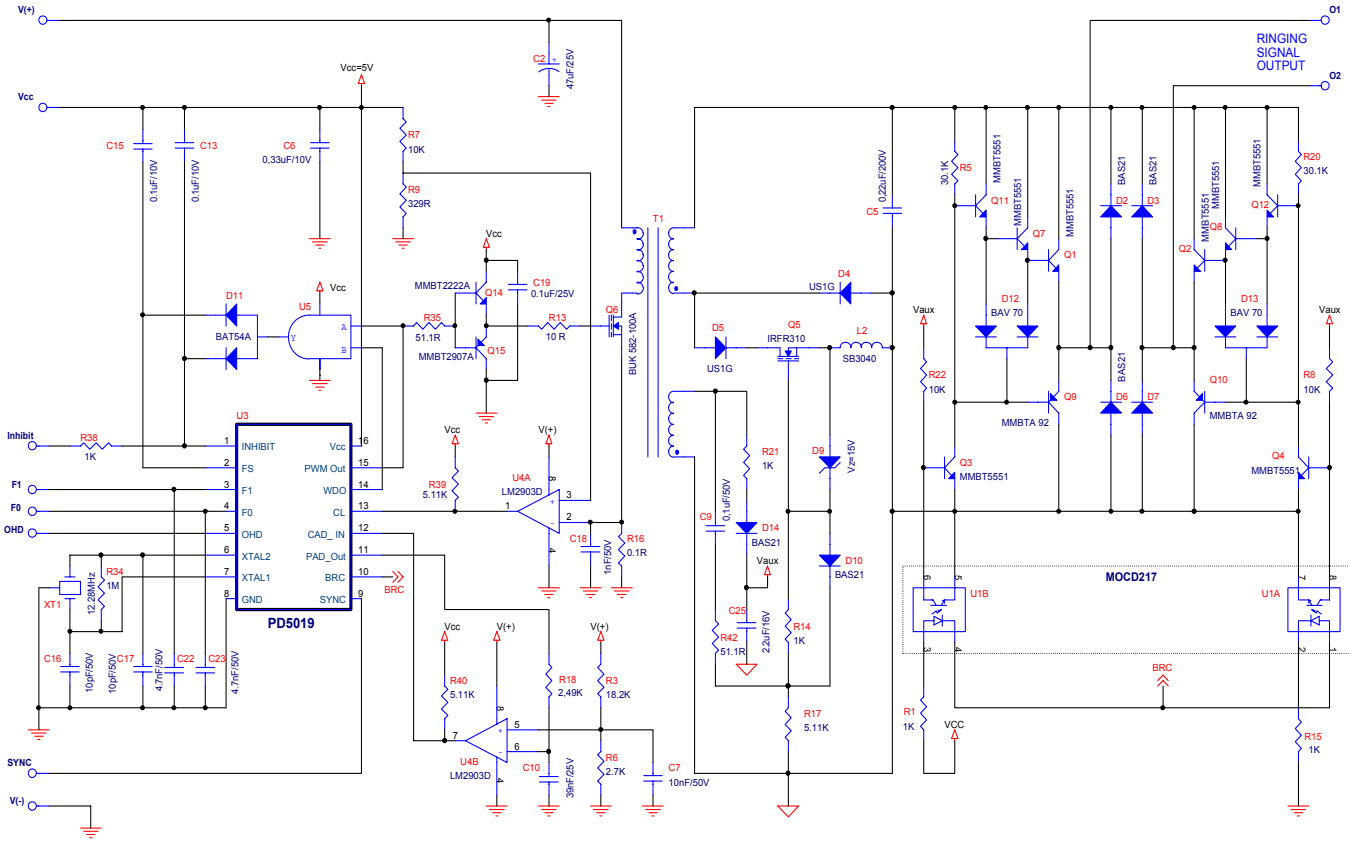
Load regulation refers to the degree of output voltage deviations as a function of output rms current variations. The load regulation capability of a ring generator built around the PD5036 will be effected by a number of design and component selection criteria:

- The quality of the transformers' primary to secondary coupling and winding leakage. Good coupling and low leakage will improve load regulation.
- Impedance of the transformer winding and core losses. Low impedance and low core losses will improve load regulation.
- Input capacitor ESR. Low ESR will reduce input voltage ripple, which will improve the input voltage A/D sampling accuracy. Since the input voltage A/D sensing directly effects the device's output voltage, high sampling accuracy will improve load regulation.
- FET dropout voltage. Low main switching and synchronous switching FETs dropout voltage will improve load regulation.
- Output bridge transistor's dropout voltage. Low dropout voltage will improve load regulation.

In proper design, load regulation of 6% for loads varying from 10% to 100%, and 10% regulation for loads varying from no load to 100% of the circuit's rated load, can be achieved. Rated load is defined as the equivalent loading that does not cause the PD5036 to decrease the ring generator's output voltage, or trigger the overload/short circuit protection.



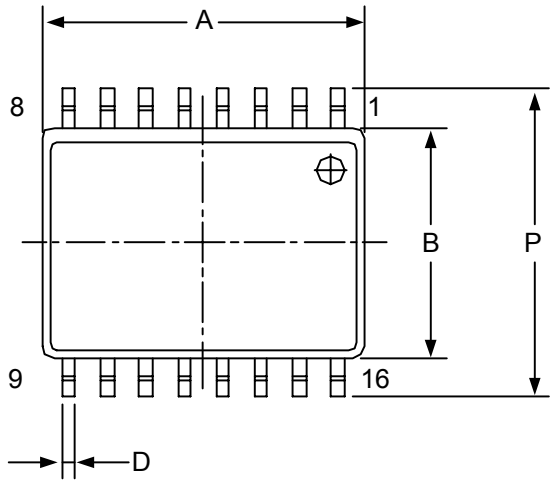
Typical Application – 2 REN Sine Wave Ring Generator



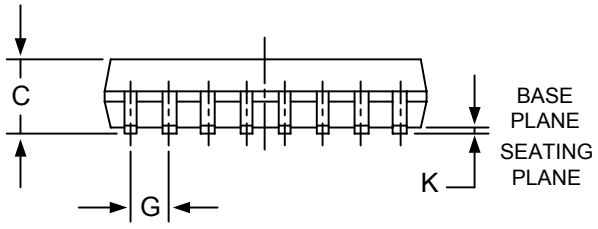
Typical Application - 3 to 6REN Sine Wave Ring Generator

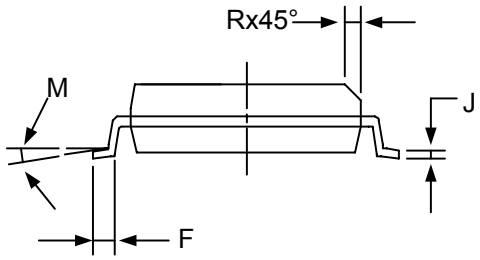
MECHANICAL DETAILS

Top View



DIM	MILLIMETERS		INCHES	
	MAX	MIN	MIN	MAX
A	10.20	10.35	.402	.408
B	7.40	7.60	.292	.298
C	2.40	2.65	.094	.104
D	0.35	0.51	.0138	.020
F	0.40	0.90	.016	.035
G	1.27 BSC		.050 BSC	
J	0.23	0.32	.0091	.0125
K	0.10	0.30	.0040	.0118
M	0°	8°	0°	8°
P	10.10	10.60	.398	.416
R	0.25	0.75	.010	.029





Notes:

1. Dimensions and tolerance per ANSI Y14.5M 1982
2. Controlling dimensions: millimeter.
3. Dimensions “A” and “B” do not include mold protrusion.
4. Maximum mold protrusion 0.15mm (0.006”) per side.
5. Dimension “D” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005”) total in excess of “D” dimension at maximum metrical condition.
6. Package type: SOW-16

PowerDsine application engineers will provide technical assistance integrating the PD5036 for customers using more than 10,000 units. For quantities lower than 10,000 units, use of a modular sine wave ring generator is recommended (PCR-SIN01A Series, PCR-SIN03B Series, or the PCR-SIN06 Series). *To receive PowerDsine PD5036 applications notes or to obtain technical assistance, please contact your local representative or PowerDsine’s main offices, detailing your application requirements.*

Distributor

PD5036- Rev02 0500

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